US005680318A

United States Patent [19]

Gregory et al.

[11] Patent Number: 5,680,318

[45] Date of Patent: Oct. 21, 1997

[54] **SYNTHESIZER FOR GENERATING A LOGIC NETWORK USING A HARDWARE INDEPENDENT DESCRIPTION**

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[21] Appl. No.: **471,060**

[22] Filed: **Jun. 6, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 632,439, Dec. 21, 1990, abandoned.

[51] **Int. Cl.**[6] **G06F 17/50**

[52] **U.S. Cl.** **364/489**; 364/490

[58] **Field of Search** 395/800; 364/489, 364/490

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,458,240	7/1969	Hanson	328/92
4,342,093	7/1982	Miyoshi	364/578
4,677,587	6/1987	Zemany, Jr.	364/900
4,703,435	10/1987	Darringer et al.	364/489
4,725,971	2/1988	Doshi et al.	364/578
4,725,975	2/1988	Sasaki	364/900
4,792,909	12/1988	Serlet	364/491
4,792,913	12/1988	Buckland	364/602
4,833,619	5/1989	Shimizu	364/489
4,882,690	11/1989	Shinsa	364/489
4,896,272	1/1990	Kurosawa	364/490

(List continued on next page.)

OTHER PUBLICATIONS

Giovanni De Micheli, *High–Level Syntheses of Digital Circuits* 6–7, IEEE Design & Test of Computers (Oct. 1990).

R. Camposano, *From Behavior to Structure: High–Level Synthesis* 8–9, IEEE Design & Test of Computers (Oct. 1990).

Giovanni De Micheli et al., *The Olympus Syntheses System* 35–53, IEEE Design & Test of Computers (Oct. 1990).

Roger Lipsett, *VHDL–The Language* 28–41, IEEE Design & Test (Apr. 1986).

Alfred S. Gilman, *HDL–The Designer Environment* 42–47, IEEE Design & Test (Apr. 1986).

Peter M. Maurer et al., *Techniques For Unit–Delay Compiled Simulation* 480–484, 27th ACM/IEEE Design Automation Conference, Paper 27.1 (1990).

Zhicheng Wang et al., *LECSIM: A Levelized Event Driven Compiled Logic Simulator* 491–496, 27th ACM/IEEE Design Automation Conference, Paper 27.3 (1990).

J. Bhasker et al., *An Optimizer For Hardware Synthesis* 20–36, IEEE Design & Test of Computers (Oct. 1990).

Raul Camposano, *Design Process Model in the Yorktown Silicon Compiler* 489–494, 25th ACM/IEEE Design Automation Conference, Paper 32.3 (1988).

(List continued on next page.)

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[57] **ABSTRACT**

A method and system are provided for generating a logic network using a hardware independent description means. A logic circuit synthesizer, in response to a user description specifying only signals and the circumstances under which the signals are produced, generates a logic network that generates the signals specified in the user description, e.g., a net list of logic elements, such as logic gates, high impedance drivers, level sensitive latches and edge sensitive flip-flops along with the interconnections of the logic elements. In one embodiment, the logic circuit synthesizer includes a preprocessor means and a logic circuit generator means. The preprocessor means, in response to the user description, converts signals and conditions in the user description into a structure having nodes interconnected by edges. The edges include an edge condition under which the edge is traversed. The logic circuit generator, using the structure and the edge conditions, creates a logic network that generates the signals specified in the user description.

50 Claims, 25 Drawing Sheets

Microfiche Appendix Included
(3 Microfiche, 205 Pages)